An Energy Efficient and Resource Optimal VLSI Architecture for ECG Feature Extraction for Wearable Healthcare Applications

Meenali Janveja*, Rushik Parmar, Gaurav Trivedi
Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, Guwahati, India
Email: ****meena176102001@iitg.ac.in***

Pidanic Jan†, Zdenek Nemec
Department of Electrical Engineering, University of Pardubice, Pardubice, Czech Republic
Email: †***jan.pidanic@upce.cz***

***Abstract*—The paper presents a low complexity algorithm for extracting features of an electrocardiogram (QRS complex, P wave and T wave). A low power and resource optimal architecture is designed to implement this algorithm efficiently. The algorithm's parameters are chosen appropriately to avoid any floating-point compute-intensive arithmetic operation enabling us to implement it using comparators, shifters and adders only, which leads to efficient hardware resource utilization. The proposed architecture employs techniques such as clock gating to optimize power consumption. The modules delineating different peaks and boundaries of the ECG signal can be turned off when they are not operational or as per the medical requirements. The algorithm and architecture proposed in this paper are validated using MIT-BIH and QT database from Physionet. The proposed algorithm is implemented using the $Virtex-7$ FPGA platform with average resource utilization of 0.42%, which is the least compared to other methods. The implementation is synthesized using $180\ nm$ CMOS technology. The proposed design utilizes $7.38\ \mu W$ and $7.38\ pJ$ of power and energy respectively, at an operating frequency of $1\ MHz$ at $1.98\ V$. The energy consumption of the proposed architecture is reduced by factor of 1.28 compared to other known methods due to minimal utilization of Flip-Flops and LUTs. Therefore, our architecture can be efficiently deployed in low power and resource-constrained wearable healthcare applications.**

***Index Terms*—ECG signal, QRS, P wave, T wave, Wearable devices.**

I. Introduction

The modern unfit lifestyle habits and inadequate medical facilities have led to an exponential increase in mortality rate. Amidst all the diseases, cardiovascular diseases (CVD) have scourged the world with millions of deaths each year [1]. An Electrocardiogram (ECG) signal is widely used by professionals worldwide to analyze different heart abnormalities. Continuous monitoring of ECG signals aids in evaluating the condition of the heart for any underlying diseases, and therefore avoiding fatalities. There is a great necessity to develop wearable devices capable of processing ECG signals in low power and small areas. The wearable devices lead to early detection of CVD, giving time to patient and doctor for life saving [2]. Recent research signifies that the use of such Internet of things (IoT) healthcare wearable devices effectively lowers the risk of casualties and the rate of hospitalization [3]. Due to their portable nature, these devices must restricted power and area resources. Therefore, ECG processing systems should be developed with stringent power and area needs. Considering these constraints, we propose a simple and efficient ECG signal analysis algorithm to extract fiducial points. Their area and power-optimized VLSI architecture is suitable for incorporating into wearable devices for monitoring ECG.

A. *State of the Art in ECG Feature Extraction*

Accurate analysis and delineation of ECG signals play a crucial role in diagnosing CVD. Therefore, ample research has been done to develop efficient algorithms and hardware for ECG feature extraction. Pan and Tompkins developed a QRS detection algorithm that has remarkable accuracy but is expensive in terms of hardware [4]. Authors in [5] developed an energy-efficient ECG signal processor to detect cardiovascular diseases such as arrhythmia, myocardial infarction and more. The work is implemented on $130\ nm$ technology utilizing $96pJ$ of energy. The cited work does not address the delineation of boundaries of the P wave and the onset of the T wave. Vemishetty et el. [6] proposed an algorithm based on wavelet transform and implemented it on $180\ nm$ technology that consumed $9.64\ pJ$ energy. Ultra-low-power hardware is proposed by Temesghen et el.; in [7] for IoT healthcare devices. It utilized a curve-length transform to mark only the R peaks while the rest of the feature extraction is not addressed. Bote et el. [8] developed a modular design in which the quality of delineation is adjusted in runtime as per medical requirements. The algorithm is processed using the $TIMSP430$ series microcontroller. These general-purpose microcontrollers could be a central processing unit for wearable healthcare devices. However, the active power dissipation of these microcontrollers is much higher than the custom ASIC processors [7]. Also, the paper utilizes morphological operations to detect the onset and offset of ECG peaks that add up to hardware resource utilization. This paper proposes an efficient and simple algorithm to extract all characteristic features of ECG waves. An area and power-optimized VLSI architecture is then designed for the proposed algorithm. The architecture is designed so that it utilizes no floating-point operations. If the complete delineation is not needed, some modules such as P and T wave block can be disabled to reduce computational load and power. These modules can be turned on if any anomaly is detected in the ECG. This

modular architecture makes it a suitable candidate for wearable healthcare devices to detect cardiovascular diseases further.
The rest of the paper is sectioned as follows. Section III describes the proposed work. Results are discussed in section IV. Section V concludes the paper.

II. Proposed Work

A. *ECG Feature Extraction Algorithm*

This section describes the proposed ECG feature extraction algorithm to detect P wave, QRS complex and T wave and mark their fiducial points (onset, offset and peak). The algorithm starts with the extraction of the QRS peak, which is the most prominent feature of an ECG wave and is used to detect a person's heart rate. Any irregularity in the occurrence of the R peak signifies cardiac arrhythmia. Later, QRS boundaries and P, T waves are delineated if any abnormality is detected in the $R-R$ interval or as per the medical requirements.
The raw ECG has motion artefacts, isoelectric line wandering and high-frequency noises with the signal components. The signal is first processed to remove these noises to ensure accuracy in extracting fiducial points. The digitized ECG signal is filtered using a band-pass filter of bandwidth $0.5-40\ Hz$ [5]. Figure 1 depicts the flow chart of the proposed algorithm.

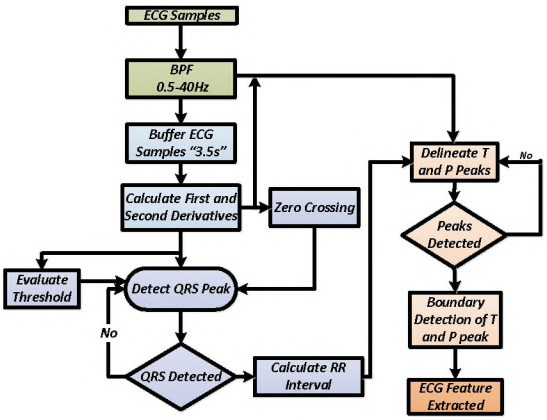

Fig. 1. Flow Chart of Proposed Algorithm

*1) **Peaks Detection Modules**:* The function of the peak detection module is to mark the R peaks and P and T peaks if required. A single and double derivative of the filtered ECG signal is taken as input to this module for performing peak detections. The shape of the QRS complex depends on the selected lead. In some leads such as $V6$, the R peak is most significant, whereas in the lead $V1$, the R peak is small and is followed by a prominent negative S peak. The proposed methodology considers the former as a positive QRS complex and the later as negative [8]. As shown in the flow chart 1, an initial window of $3.5\ s$ is considered for processing the ECG signal. Later, the filtered ECG signal's single and double derivative is computed to extract the QRS peak. Once the double derivative is obtained, an absolute maximum (abs_max) value of the double derivative signal (ECG'') is calculated for the considered $3.5\ s$ window. The threshold is then computed to detect the R peaks according to equation 1.

$$th_R = abs\_max/4 \tag{1}$$

R peak is marked if a zero crossing is encountered and a magnitude of ECG'' is greater than the described threshold. If the value of ECG'' is positive, then a positive QRS peak is considered; else, it is considered as negative QRS complex. The threshold for finding R peaks is updated with every $3.5\ s$ window making the detection adaptive to the uneven heartbeat. $R-R$ intervals (RR) are computed along with detecting the R peaks. The duration of the QRS complex is $120\ ms$. Therefore, if the found R peak is positive, then the Q and S peak is marked as the minimum value in the window of $60\ ms$ before and after the R peak, respectively. When the detected QRS complex is negative, the R peak is marked as the maximum value in a $60\ ms$ window before the obtained negative peak. The negative peak will then be marked as S peak. Once the R peaks are estimated, the RR intervals are calculated as the difference between consecutive R peaks.

Further, P and T peaks are calculated, if required, after delineating the respective R peaks. The P wave is the first feature of the ECG wave whose average duration is shorter than $120\ ms$. However, in patients with atrial fibrillation, its duration can be up to $170\ ms$ [9]. Therefore, a window less than $170\ ms$ before the R peak is considered for delineating the P peak. Maximum and minimum of the second derivative of the ECG signal are found in a chosen window. If the minimum magnitude is greater than the maximum in a given window, then a P wave is considered positive; otherwise, it is negative. The value of the ECG sample corresponding to the minimum of ECG'' is marked as a P peak for positive P wave and vice versa for the negative P wave. If the absolute value of the minimum or the maximum is less than 1% of abs_max as described above, then the P peak is not annotated. The final feature of an ECG wave is the T wave. In a normal individual, duration of a T wave varies from $125-200\ ms$ [9]. However, it varies when a person is suffering from cardiac issues. Therefore, a similar approach as the P wave is used to extract a T peak after chosing a window of $200\ ms$ after the delineated R peaks. The heartbeat (HB) can also be found using equation 2. f_S is the sampling rate of the ECG signal.

$$HB = 60 \times (\frac{f_s}{RR\ interval}) \tag{2}$$

*2) **Boundary Detection Module**:* Once the R peak is detected, the onset and offset of ECG peaks can be described. The boundaries of $P-QRS-T$ waves are detected using the zero slope criteria. A suitable window is considered following the standard duration of the respective waves before and after the previously found peak. Once the window is defined, sample values with zero slopes before a peak are marked as onset and after as an offset. However, there may be cases when

no samples with zero slope are obtained. To delineate the boundaries in such conditions a sample value smaller than 5% of the respective peak value is marked as the boundary of a considered peak in given windows. Both the procedures are considered for reliable feature extraction of ECG waves.

B. *Hardware Implementation*

As shown in figure 1, the proposed algorithm has two main blocks; peak detection and boundary detection. Among them, the R peak block is mandatory, whereas other sub-blocks are optional and operational as medical requirements.

The proposed algorithm is implemented in hardware as a finite state machine in Verilog HDL using Xilinx Inc's Vivado 2019 development environment. Figure 2 represents the state machine that controls the operation of different blocks.

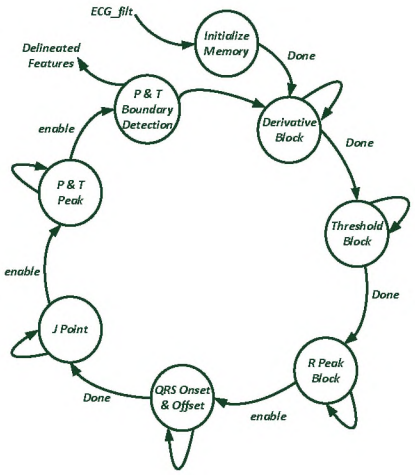

Fig. 2. Finite State Machine of Proposed Architecture

Initially, ECG signals sampled at $250\ Hz$ and filtered at a specified frequency of $0.5 - 40\ Hz$ are fed serially to the architecture as explained above. Each ECG sample is considered to be of 11 bits. As it is known that floating-point operations are complex to perform in hardware and utilize additional resources, integer representations of ECG signals are considered. ECG samples are available in the double-precision format; they are first converted into integer format by multiplying them by a factor of 100. Further, these ECG samples are rounded to their integer values, avoiding the floating-point arithmetic. It is observed that multiplying each sample by a factor of 100 gives negligible variation in the interbeat interval of the ECG signal. A memory is first initialized that stores the filtered ECG samples, which will be utilized later to mark the position of the ECG features. The filtered ECG samples are then fed to the differentiator block serially which calculates the single derivative (ECG') and double derivative (ECG'') output of the ECG signal. The double derivative output is fed as input to the threshold block. As shown in equation 1, the divide by 4 operation in threshold for R peak delineation (th_R) can be calculated as a shift by 2 operation $(>> 2)$. Further, the R peak position can be marked using a simple comparator circuit. Later, all the window sizes and threshold required to estimate P and T waves are taken to avoid any floating-point arithmetic. This aids in optimizing the hardware resources and reduces computational complexity making the overall architecture simple. The functionality of

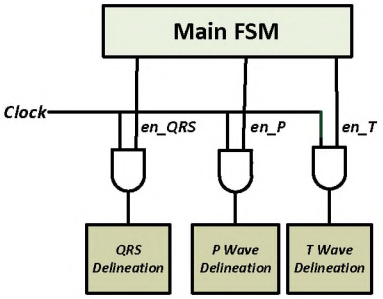

Fig. 3. Clock Gating Utilized in the Proposed Architecture

architecture is divided into several blocks which are controlled by the clock and enable signal. The R peak is the first feature delineated once the signal's double derivative is obtained. Once the R peak is obtained, the modules to examine other features are clock gated to optimize power. Therefore, the proposed architecture is suitable for deploying in resource-constrained wearable healthcare ECG analysis applications. Their key requirement is real-time analysis of ECG signals for any anomalies in the power and resource-constrained environment.

III. Results and Discussion

This section elaborates the experimentations performed and output obtained from the proposed methodology.

A. *Validation of Algorithm*

The proposed algorithm is first implemented in Python to validate its functionality. It is then verified on ECG experts taken from $MIT - BIH$ and QT database of Physionet [10]. The $MIT - BIH$ database consists of 48 half-hour excerpts of two-channel ambulatory ECG recordings sampled at $360\ Hz$. The experts are downsampled at $250\ Hz$ for use in the proposed algorithm. The QT dataset contains $105\ 15min$ excerpts of 2-lead ECG recordings sampled at $250\ Hz$. Figure 4 displays the delineated features on MIT-BIH dataset(106) using Python. The experts are first annotated manually with guidance of an expert for verification. For every ECG signal, a comparison of manual and algorithmic annotated features is performed. It is observed that the proposed algorithm delineates in proximity of $150\ ms$ of the manually annotated signal. This error metric of ECG feature extraction is described by the Association for the Advancement of Medical Instrumentation (AAMI) [11] for verification of the ECG feature extarction algorithm.

When a feature is delineated correctly, *True Positive*(TP) is counted, and the respective error is calculated between manual and algorithmically annotated features. A *False Negative*(FN) is considered if no features are detected. If a point is not

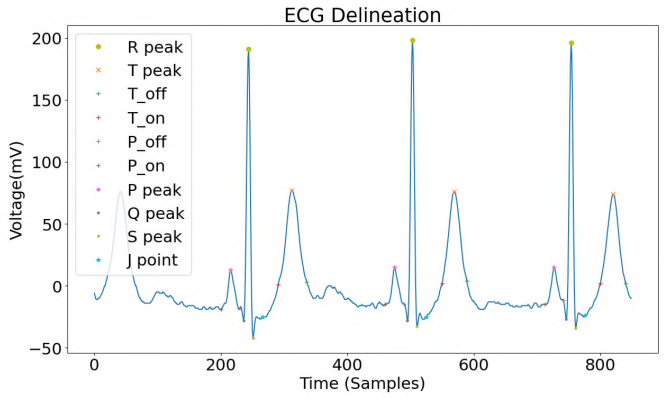

Fig. 4. Extracted ECG Features of MIT-BIH dataset(106)

related to any annotated feature, it is regarded as *False Positive*(FP). Considering these basis, *Sensitivity*$(Se\%)$ and *Positive Predicted Value*$(PPV\%)$ metrics are defined for the performance evaluation of the proposed algorithm in equation 3.

$$Se\% = \frac{TP}{TP + FN}$$
$$PPV\% = \frac{TP}{TP + FP} \tag{3}$$

Table I presents the test result of the proposed algorithm on ECG excerpts from QT dataset [10].

TABLE I
COMPARISON OF ECG FEATURE EXTRACTION RESULTS ON QT DATABASE

Algorithm	Implementation Platform	Metric	P Wave	QRS Wave	T Wave
Bote et al. [8]	TI MSP430 series microcontroller	Se%	98.23	99.88	98.18
		PPV%	94.38	99.41	96.39
Rincon et al. [12]	Shimmer TM embedded platform	Se%	99.88	99.97	99.97
		PPV%	92.04	98.66	98.70
Di Marco et al. [13]	Software	Se%	98.15	100	99.72
		PPV%	91.00	-	97.76
Sanjeev et al. [5]	ASIC	Se%	98.91	100	99.97
		PPV%	91.07	100	97.76
Kalyakulina et al. [14]	Software	Se%	97.49	98.42	97.2
		PPV%	97.89	98.24	96.55
Proposed Work	FPGA	Se%	98.84	99.86	99.12
		PPV%	96.33	99.56	97.86

It is observed that the proposed algorithm is much less complex than the algorithms proposed in [5], [8], [13], [14] and [12]. Moreover,it is observed from table I that the proposed algorithm displays an equivalent or better sensitivity in extracting the features of an ECG compared to the literature; verifying the algorithm's efficacy. Moreover, the computational simplicity of the proposed algorithm makes it a suitable candidate for low power real-time ECG analysis applications due to the area and power-optimized hardware implementation. Robust QRS extraction is achieved using the double derivative of the ECG signal with added adaptive threshold and detection windows. The sensitivity of 99.86% and positive predictivity of 99.56% is attained to detect the QRS complex that comprises the peak and boundary detection. The QRS peak is marked as a reference point to delineate other features such as the P and T waves and intervals such as the $R-R$ interval. Moreover, proposed algorithm demonstrates a comparable sensitivity for the P and T wave extraction as evident from table I.

TABLE II
COMPARISON OF FPGA IMPLEMENTATION OF R PEAK DETECTION

Architecture	Available LUT	LUT Utilized	% Utilization	Available FF	FF Utilized	% Utilization	Total % Utilization
[15]	9312	3443	24%	4656	2901	62%	45.4%
[16]	9312	3061	32%	4656	1809	38%	34.86%
[17]	124467	3734	3%	34240	1712	5%	3.43%
[18]	9312	2328	20%	4656	1489	32%	27.3%
[19]	12480	1408	11%	12480	1086	8%	9.99%
[20]	303600	88456	29%	607200	5728	0.94%	10.34%
Proposed	303600	422	0.13%	607200	293	0.05%	0.08%

B. *Hardware Implementation Results*

The proposed work is implemented in hardware using Verilog, and the modules are simulated for functionality in the Xilinx 2019 Vivado development environment. Later, the modules are verified using the Xilinx Virtex-7 FPGA board. For validating the proposed architecture, multiple test-bench as different ECG signal experts [10] are created to verify the outcome of the proposed algorithm with the Python implementation and manual annotations. It is observed that the outcome of the extracted features from the architecture is in close correlation with the software annotations and the manual readings.

The QRS complex is the most critical feature of an ECG wave, and hence, various methods have been reported in the literature for delineation of the R peak only. Therefore, for completeness, the R peak module of the proposed architecture is implemented first, and its hardware resources are evaluated and compared with some previous works in table II. It is observed that the proposed architecture utilized only 0.1% of available resources on Virtex-7 FPGA to find the QRS peaks, which is the least among the literature.

Later, architecture for complete ECG delineation is implemented on FPGA and hardware resource utilization is realized. Table III presents the resources utilized by the proposed architecture for complete ECG feature extraction. It is seen that the architecture uses only 0.42% of total available resources available on Virtex-7 FPGA. On comparing this work with the literature in table IV, it is observed that the proposed architecture utilized only 2409 lookup tables and 1230 flip-flops. The resource utilization is approximately 11 times better than the most efficient method reported in [21], making the proposed architecture efficient and well-optimized as it employs the least available resources.

Further, the entire design is synthesized in $180\ nm$ CMOS technology to reckon the power consumption of the architecture. The proposed design is compared with other state-of-the-art methods, which are also designed using the $180\ nm$ technology node for fair comparison in table V.

TABLE III
FPGA IMPLEMENTATION OF COMPLETE ECG FEATURE EXTRACTION ARCHITECTURE (XILINX VIRTEX-7 FPGA)

Resource	Available	Utilization	Percentage Utilization(%)
LUT	303600	2409	0.79
FF	607200	1230	0.20
DSP	2800	11	0.39
IO's	700	233	38.83
BRAM	1030	1.50	0.15

TABLE IV
COMPARISON OF FPGA IMPLEMENTATION OF COMPLETE ECG FEATURE EXTRACTION

Architecture	LUT			Flip Flop		
	Available	Utilized	Percentage Utilization(%)	Available	Utilized	Percentage Utilization(%)
[22]	40960	29389	71	20480	15459	75
[23]	343680	119256	34.7	687360	130598	19
[24]	239616	131072	55	18752	3532	19
[21]	69120	24784	35	69120	14670	21
Proposed	303600	2409	0.79	607200	1230	0.20

TABLE V
POWER COMPARISON OF SYNTHESIS RESULTS

Parameter	[25]	[26]	[27]	[28]	Proposed Work
Technology	180nm	180nm	180nm	180nm	180nm
Operating Frequency	1 MHz	1 MHz	NA	0.12 KHz	1 MHz
Supply Voltage	1.8V	1.2V	1.0V	1.2V	1.98V
ECG Features	P-QRS-T	P-QRS-T	QRS	QRS	P-QRS-T
Power	$9.47\mu W$	$32\mu W$	$0.410\mu W$	$5.97\mu W$	$7.38\mu W$
Energy	9.47pJ	32pJ	NA	49.75nJ	7.38pJ

The proposed algorithm consumes a mere $7.38\ \mu W$ of power when operated at $1\ MHz$ at an operating voltage of $1.98\ V$, which is less when compared to the literature in [25], [26]. However, the architectures in [27], and [28] utilized $0.410\ \mu W$ and $5.97\ \mu W$ of power, respectively, which is less when compared to the proposed design. However, it should be noted that the architecture of [27] and [28] reports only QRS detection and thus has fewer architectural requirements than our proposed architecture which is designed to perform complete $P-QRS-T$ feature extraction. Also, they are operated at lower frequency and voltage, leading to less power consumption. Moreover, the proposed architecture is compared in terms of energy with the mentioned state-of-the-art works for a better comparison. It can be concluded from table V that the proposed design has the least energy requirements $(7.38\ pJ)$ compared to other architectures. Therefore, based on the hardware implementation results, it is summarised that the proposed design consumes low power and hardware resources, making it suitable for low power wearable healthcare applications.

IV. CONCLUSION

This paper presents a low complexity algorithm and its area and power efficient VLSI architecture for ECG feature $(P-QRS-T)$ extraction. An average sensitivity of 99% is achieved on the QT dataset by the proposed algorithm, comparable or better than previous literature. The algorithm utilized simple difference and comparison operations, avoiding all floating-point calculations to delineate the features, making it computationally inexpensive. The proposed design incorporates the technique of clock gating to control the operability of the different modules optimizing the power requirements. The proposed algorithm is implemented in Verilog using the Xilinx FPGA development platform. Since the QRS complex is the most prominent feature of an ECG wave, most heart anomalies can be observed by reckoning the variation in the position and the value of R peaks. Therefore, the architecture was first developed to extract the R peak, which only utilized an average 0.1% hardware resources. Then the architecture is designed to delineate a complete ECG feature set, and it uses an average of 0.42% of hardware resources which is the least among similar state-of-the-art architectures. The presented architecture is then synthesized using $180\ nm$ CMOS process technology to evaluate its power requirements. The architecture utilizes $7.38\ pJ$ of energy, which is the least compared to other reported architectures in the literature. Therefore, the proposed architecture could be considered viable for employment in low power and resource-constrained application of wearable devices.

V. ACKNOWLEDGEMENT

The work has been supported from the programme INTER-EXCELLENCE (LTAIN19100) funds of the Ministry of Education, Youth and Sports, Czech Republic, project LTAIN19100 "Artificial Intelligence Enabled Smart Contactless Technology Development for Smart Fencing". This support is very gratefully acknowledged.

REFERENCES

[1] W. H. Organization, *World health statistics 2015*. World Health Organization, 2015.

[2] S. M. Grundy, G. J. Balady, M. H. Criqui, G. Fletcher, P. Greenland, L. F. Hiratzka, N. Houston-Miller, P. Kris-Etherton, H. M. Krumholz, J. LaRosa *et al.*, "Primary prevention of coronary heart disease: guidance from framingham: a statement for healthcare professionals from the aha task force on risk reduction," *Circulation*, vol. 97, no. 18, pp. 1876–1887, 1998.

[3] A. L. Bui and G. C. Fonarow, "Home monitoring for heart failure management," *Journal of the American College of Cardiology*, vol. 59, no. 2, pp. 97–104, 2012.

[4] J. Pan and W. Tompkins, "Real time algorithm detection for qrs," *IEEE Trans. Eng. Biomed Eng*, vol. 32, no. 3, pp. 230–236, 1985.

[5] S. K. Jain and B. Bhaumik, "An energy efficient ecg signal processor detecting cardiovascular diseases on smartphone," *IEEE transactions on biomedical circuits and systems*, vol. 11, no. 2, pp. 314–323, 2016.

[6] N. Vemishetty, P. Patra, P. K. Jha, K. B. Chivukula, C. K. Vala, A. Jagirdar, V. Y. Gudur, A. Acharyya, and A. Dutta, "Low power personalized ecg based system design methodology for remote cardiac health monitoring," *IEEE Access*, vol. 4, pp. 8407–8417, 2016.

[7] T. Tekeste, H. Saleh, B. Mohammad, and M. Ismail, "Ultra-low power qrs detection and ecg compression architecture for iot healthcare devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 2, pp. 669–679, 2018.

[8] J. M. Bote, J. Recas, F. Rincón, D. Atienza, and R. Hermida, "A modular low-complexity ecg delineation algorithm for real-time embedded systems," *IEEE journal of biomedical and health informatics*, vol. 22, no. 2, pp. 429–441, 2017.

[9] G. S. Wagner, *Marriott's practical electrocardiography*. Lippincott Williams & Wilkins, 2001.

[10] A. L. Goldberger, L. A. Amaral, L. Glass, J. M. Hausdorff, P. C. Ivanov, R. G. Mark, J. E. Mietus, G. B. Moody, C.-K. Peng, and H. E. Stanley, "Physiobank, physiotoolkit, and physionet: components of a new research resource for complex physiologic signals," *circulation*, vol. 101, no. 23, pp. e215–e220, 2000.

[11] A. for the Advancement of Medical Instrumentation *et al.*, "Testing and reporting performance results of cardiac rhythm and st segment measurement algorithms," *ANSI/AAMI EC38*, vol. 1998, 1998.

[12] F. Rincón, J. Recas, N. Khaled, and D. Atienza, "Development and evaluation of multilead wavelet-based ecg delineation algorithms for embedded wireless sensor nodes," *IEEE Transactions on Information Technology in Biomedicine*, vol. 15, no. 6, pp. 854–863, 2011.

[13] L. Y. Di Marco and L. Chiari, "A wavelet-based ecg delineation algorithm for 32-bit integer online processing," *Biomedical engineering online*, vol. 10, no. 1, p. 23, 2011.

[14] A. I. Kalyakulina, I. I. Yusipov, V. A. Moskalenko, A. V. Nikolskiy, A. A. Kozlov, N. Y. Zolotykh, and M. V. Ivanchenko, "Finding morphology points of electrocardiographic-signal waves using wavelet analysis," *Radiophysics and Quantum Electronics*, vol. 61, no. 8-9, pp. 689–703, 2019.

[15] M. Karim *et al.*, "Novel simple decision stage of pan & tompkins qrs detector and its fpga-based implementation," in *Second International Conference on the Innovative Computing Technology (INTECH 2012)*. IEEE, 2012, pp. 331–336.

[16] S. Agarwal, A. Rani, V. Singh, and A. P. Mittal, "Performance evaluation and implementation of fpga based sgsf in smart diagnostic applications," *Journal of medical systems*, vol. 40, no. 3, p. 63, 2016.

[17] A. Page, A. Kulkarni, and T. Mohsenin, "Utilizing deep neural nets for an embedded ecg-based biometric authentication system," in *2015 IEEE Biomedical Circuits and Systems Conference (BioCAS)*. IEEE, 2015, pp. 1–4.

[18] H. Zairi, M. Kedir-Talha, S. Benouar, and A. Ait-Amer, "Intelligent system for detecting cardiac arrhythmia on fpga," in *2014 5th International Conference on Information and Communication Systems (ICICS)*. IEEE, 2014, pp. 1–5.

[19] M. A. Kumar and K. M. Chari, "Efficient fpga-based vlsi architecture for detecting r-peaks in electrocardiogram signal by combining shannon energy with hilbert transform," *IET Signal Processing*, vol. 12, no. 6, pp. 748–755, 2018.

[20] D. Panigrahy, M. Rakshit, and P. Sahu, "Fpga implementation of heart rate monitoring system," *Journal of medical systems*, vol. 40, no. 3, p. 49, 2016.

[21] G. G. C. Lee, Z.-J. Huang, C.-Y. Chen, and C.-F. Chen, "Implementation of gabor feature extraction algorithm for electrocardiogram on fpga," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2015, pp. 798–801.

[22] H. Chatterjee, M. Mitra, and R. Gupta, "Real–time detection of electrocardiogram wave features using template matching and implementation in fpga," *International Journal of Biomedical Engineering and Technology*, vol. 17, no. 3, pp. 290–313, 2015.

[23] X. Wang, Y. Zhu, Y. Ha, M. Qiu, and T. Huang, "An fpga-based cloud system for massive ecg data analysis," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 3, pp. 309–313, 2016.

[24] D. Alhelal, K. A. Aboalayon, M. Daneshzand, and M. Faezipour, "Fpga-based denoising and beat detection of the ecg signal," in *2015 Long Island Systems, Applications and Technology*. IEEE, 2015, pp. 1–5.

[25] N. Vemishetty, P. Patra, P. K. Jha, K. B. Chivukula, C. K. Vala, A. Jagirdar, V. Y. Gudur, A. Acharyya, and A. Dutta, "Low power personalized ecg based system design methodology for remote cardiac health monitoring," *IEEE Access*, vol. 4, pp. 8407–8417, 2016.

[26] H. Kim, S. Kim, N. Van Helleputte, A. Artes, M. Konijnenburg, J. Huisken, C. Van Hoof, and R. F. Yazicioglu, "A configurable and low-power mixed signal soc for portable ecg monitoring applications," *IEEE transactions on biomedical circuits and systems*, vol. 8, no. 2, pp. 257–267, 2013.

[27] P. Li, X. Zhang, M. Liu, X. Hu, B. Pang, Z. Yao, H. Jiang, and H. Chen, "A 410-nw efficient qrs processor for mobile ecg monitoring in 0.18-μm cmos," *IEEE Transactions on biomedical circuits and systems*, vol. 11, no. 6, pp. 1356–1365, 2017.

[28] S.-Y. Lee, J.-H. Hong, C.-H. Hsieh, M.-C. Liang, S.-Y. C. Chien, and K.-H. Lin, "Low-power wireless ecg acquisition and classification system for body sensor networks," *IEEE journal of biomedical and health informatics*, vol. 19, no. 1, pp. 236–246, 2014.